

In the Drawings

Annexed hereto is one Replacement Sheet containing amended FIG. 8 and amended FIG.

9.

REMARKS

Claims 1, 3-13, 15-19, 26, 27, 29 and 32-38 are pending in the application and stand rejected. Reconsideration of the claim rejections and drawing objections is requested in view of the following remarks.

Drawing Objections

FIGs. 8 and 9 of the drawings have been amended in the manner suggested by the Examiner. Therefore, withdrawal of the drawing objection is requested.

Claim Rejections - 35 U.S.C. §101

Claims 1, 3-13, 15-19, 26, 27, 29 and 32-38 stand rejected on the grounds that the claimed inventions as a whole do not accomplish a practical application and are directed to abstract ideas. Applicants traverse the rejection and contend that at the very least, claims 1, 10, 26 and 27 are undoubtedly directed to statutory subject matter. The Office Action is devoid of any reasonable showing, legally or factually, that supports the Examiner's finding of the claimed subject matter being directed to non-statutory subject matter.

In formulating the rejections, the Examiner fails to follow the guidelines set forth in MPEP 2106. As noted in section 2106 II A of the M.P.E.P.:

A process that consists solely of the manipulation of an abstract idea is not concrete or tangible. . . Office personnel have the burden to establish a *prima facie* case that the claimed invention as a whole is directed to solely an abstract idea or to manipulation of abstract ideas or does not produce a useful result. Only when the claim is devoid of any limitation to a practical application in the technological arts should it be rejected under 35 U.S.C. 101. . . . Further, when such a rejection is made, Office personnel must expressly state how the language of the claims has been interpreted to support the rejection. (Emphasis added.)

Moreover, as set forth in various portions of MPEP 2106 (II) (C), the Examiner must first determine the scope of a claim by thoroughly analyzing the language of the claim before

determining if the claim complies with each statutory requirement for patentability. When evaluating the scope of a claim, every limitation in the claim must be considered. The Examiner may not dissect a claimed invention into discrete elements and then evaluate the elements in isolation. Instead, the claim as a whole must be considered.

The Examiner's rejection of claims 1 and 10 are erroneous. One *fundamental flaw* in the 101 rejections is that the Examiner fails to consider the claim language of claims 1 and 10 in the entirety. On a general level, claims 1 and 10 are directed to methods for characterizing device mismatch in a semiconductor integrated circuit *by obtaining DC voltage characteristic data* for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN} , and *using the DC voltage characteristic data* to determine a distribution of device mismatch between the first and second semiconductor transistor devices.

In formulating the rejection of claims 1 and 10, the Examiner only considers the "final step of processing" of claim 1 and the "final step of characterizing" in claim 10, contending that such steps do *not produce a useful concrete and tangible result but is instead a result of internal data manipulation that is not externally conveyed*. This analysis is legally erroneous on its face as the Examiner fails to consider the claimed invention as a whole. Indeed, with regard to claims 1 and 10, the Examiner's has not fairly explained how the claimed inventions, as a whole, are not limited to practical applications within the technological arts.

In any event, when the claims are properly construed in view of Applicants' specification and in the perspective of one of ordinary skill in the art, it should be readily clear that the claimed inventions are directed to processes that undoubtedly produce a concrete tangible result of characterizing device mismatch of transistor pairs in an integrated circuit using DC voltage

characteristic data associated with the transistor pairs. The Examiner has not shown, and cannot reasonably contend, that the claimed inventions of claims 1 and 10, as a whole, are not directed to a practical application.

With regard to claims 26 and 27, the above arguments equally apply. Furthermore, in addressing claims 26 and 27, the Examiner fails to consider that the claimed inventions of claims 26 and 27 are directed to *a program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit*. In this regard, the Examiner's analysis and findings are not on point as the claimed inventions are directed NOT to a process, per se, but rather a device- a program storage device having instructions for performing the claimed process steps.

As explained in MPEP 2106(IV)(B)(1), descriptive material can be characterized as either "*functional descriptive material*" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized. Here, at the very least, claims 26 and 27 are properly viewed as being directed to program storage devices having functional description material recorded thereon, and are thus, directed to statutory subject matter.

For at least the above reasons, claims 1, 10, 26 and 27 are clearly directed to statutory subject matter. Claims 3-9, 11-13, 15-19, 29 and 32-38 are directed to statutory subject matter at

least for the same reasons given for claims 1, 10, 26 and 27. In this regard, the 101 rejections should be withdrawn.

Claim Rejections - 35 U.S.C. §103

The following obviousness rejections are asserted:

- (i) Claims 1, 3, 5-10, 12, 26, 27, 29 and 32 were rejected as being unpatentable over U.S. Patent No. 6,275,094 to Cranford in view of Conti;
- (ii) Claim 4 stands rejected as being unpatentable over Cranford in view of U.S. Patent No. 6,731,916 to Haruyama;
- (iii) Claims 13 and 33 stand rejected as being unpatentable over Cranford in view of Conti and further in view of U.S. Patent No. 5,999,043 to Zhang et al;
- (iv) Claims 11 and 34 stand rejected as being unpatentable over Cranford in view of Conti and further in view of Zhang and further in view of U.S. Patent No. 6,819,183 to Zhou et al.;
- (v) Claims 15, 16, 35 and 36 stand rejected as being unpatentable over Cranford in view of Conti and further in view of U.S. Patent No. 4,851,768 to Yoshizawa et al;
- (vi) Claim 18 stands rejected as being unpatentable over Cranford in view of Conti and further in view of U.S. Patent No. 6,181,621 to Lovett; and
- (vii) Claims 19 and 38 stand rejected as being unpatentable over Cranford in view of Conti and further in view of U.S. Patent No. 6,798,278 to Ueda.

The above rejections are all traversed for at least the same reasons provided in the previous Amendment filed on May 2, 2006, which is incorporated herein by reference. However, Applicants will address some points of contention raised in the Response to Arguments on page

17, et seq. of the Office action, as well as some salient points regarding the impropriety of the claim rejections. Out the outset, it appears that the crux of the rejections is seemingly based on the Examiners misunderstanding, or outright lack of understanding, of the claimed subject matter. Indeed, this is evidenced by each claim rejection being preceded by “as may best be understood”, as well as the continued misunderstanding as to the difference between DC current and DC voltage. If the Examiner is having difficulty in understanding the subject matter of the claimed inventions, it is requested that the Examiner contact the undersigned attorney for clarification.

In general, the crux of the rejections is based on clear misinterpretations and mischaracterizations of the teachings of Cranford and Conti as applied to the claimed inventions. For example, the Examiner’s reliance on the unrelated teachings of Cranford is bewildering as Cranford is directed to a method for dynamically adjusting the threshold voltage of a CMOS device in a receiver to provide improved noise margin and to a method for dynamically matching the threshold voltages in a differential amplifier to correct for manufacturing offset (See Abstract).

The Examiner’s attempt to explain the rejection of claim 1 (Office Action, page 18, et seq.) with regard to Cranford is unclear and glaringly fails to consider the claim language. For instance, the Examiner contends, without support, that Cranford in Col. 8, lines 1-4, in conjunction with FIG. 8 *clearly describes that the output voltage obtained from the common node connection between the first and second transistor devices comprises a DC voltage corresponding to device mismatch*. However, Col. 8, lines 1-4 of Cranford states that:

FIG. 8 shows the change in various harmonics in the output signal 163 after the offset voltage supplied by the feedback circuit 150 is provided to the transistors connected to the output terminal 116, 120 (see FIG. 5).

The Examiner does not explain how this is even remotely related to the invention of claim 1. Indeed, at the very least, the Examiner fails to address the claim language of claim 1 which recites, in part, obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN} , wherein V_{IN} is applied to a gate of at least one of the first and second semiconductor transistor devices and wherein V_{OUT} is obtained at a common node connection of the first and second semiconductor transistor devices . . . Notwithstanding the lack of explanation, FIG. 8 is nothing more than a representation of the offset in FIG. 7 in terms of amplitude and frequency for the various harmonics in the output signal prior to correction of offset voltage (see, Col. 5, lines 4-6). In other words, FIG. 8 illustrates Amplitude (in db) of the output signal as a function of Frequency (i.e., Output Voltage Amplitude vs. Frequency).

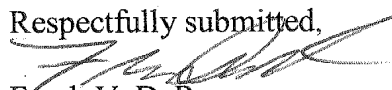
In stark contrast, as clearly recited in the claimed inventions, the DC voltage characteristic data for a device pair comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN} . In this regard, the Examiner cannot reasonably argue that FIG. 8 of Cranford discloses DC voltage V_{OUT} as a function of an input DC voltage V_{IN} , especially given the clear explicit teachings of Cranford as to what FIG. 8 represents. In this regard, the Examiner's arguments as premised on Cranford are fundamentally flawed on both technical and legal grounds.

Moreover, it could not be any more clear that the Examiner's reliance on Conti in support of the claim rejections is grossly misplaced as Conti teaches a mismatch model based on measurements of drain current I_D (see page 173, second column on bottom). The Examiner continues to misunderstand the *fundamental difference* between **DC Voltage characteristic data** (as claimed) and **DC Current characteristic data** (as disclosed in Conti). The Examiner should

review pages 6-9 of the Background section of Applicants' specification, which explains the problems associated with the use of DC current characteristic data for purposes of evaluating device mismatch.

Since all 103 rejections are essentially based on the primary combination of Cranford and Conti as applied to claims 1, 10 , 26 and 27, the rejections are legally defective on their face for at least those reasons given above. Accordingly, withdrawal of the obviousness rejections is requested.

Respectfully submitted,



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